AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A data processing apparatus comprising:

an instruction memory in which an instruction is stored;

a data memory in which data is stored;

an instruction decoder decoding a fetched instruction,

a memory operation unit ~~connected~~ coupled to said instruction memory, said data memory and said instruction decoder, fetching an instruction stored in said instruction memory, and accessing said data memory according to a decode result of said instruction decoder; and

an integer operation unit carrying out an integer operation according to a decode result of said instruction decoder,

said instruction memory including a plurality of instruction memory banks,

said memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle and a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks ~~instruction readout only from said selected instruction memory bank without reading out any instructions from unselected instruction banks~~ to carry out low power consumption pipeline processing when a plurality of instructions are fetched from the plurality of instruction memory banks.

2. (Original) The data processing apparatus according to claim 1, wherein said instruction memory further includes a first bank select circuit decoding an address including a low order address to generate chip select signals of said plurality of instruction memory banks

so that a different instruction memory bank of said plurality of instruction memory banks is accessed when instructions at continuous addresses are accessed.

3. (Previously Presented) The data processing apparatus according to claim 1, wherein said instruction memory further includes a high speed instruction memory,

wherein said memory operation unit generates a pipeline cycle corresponding to instruction readout to carry out a pipeline process when fetching an instruction from said high speed instruction memory.

4. (Previously Presented) The data processing apparatus according to claim 1, wherein said data memory includes a plurality of data memory banks,

wherein said memory operation unit generates a pipeline cycle corresponding to selection of a data memory bank and a pipeline cycle corresponding to data access to carry out a pipeline process when accessing said plurality of data memory banks.

5. (Original) The data processing apparatus according to claim 4, wherein said data memory further includes a second bank select circuit decoding an address including a high order address to generate chip select signals of said plurality of data memory banks in order to divide said plurality of data memory banks into two different regions.

6. (Original) The data processing apparatus according to claim 5, wherein said second bank select circuit decodes an address including a low order address to generate chip select signals of said plurality of data memory banks so that a different data memory bank in said

plurality of data memory banks is accessed when data at continuous addresses in said two different regions are accessed.

7. (Previously Presented) The data processing apparatus according to claim 4, wherein said data memory further includes a high speed data memory,

wherein said memory operation unit generates a pipeline cycle corresponding to data access to carry out a pipeline process when accessing said high speed data memory.

8. (Original) The data processing apparatus according to claim 1, wherein said memory operation unit fetches an instruction from said instruction memory via an instruction bus and accesses said data memory via a data bus differing from said instruction bus.

9. (Original) The data processing apparatus according to claim 1, wherein said memory operation unit reads out data from said data memory via a data input bus, and writes data into said data memory via a data output bus differing from said data input bus.

10. (Currently Amended) A data processing apparatus comprising:

an instruction memory in which an instruction is stored;

a data memory in which data is stored;

an instruction decoder decoding a fetched instruction;

a register file;

a memory operation unit ~~connected~~ coupled to said instruction memory, said data memory and said instruction decoder, fetching an instruction stored in said instruction

memory, and accessing said data memory according to a decoded result of said instruction decoder; and

an integer operation unit carrying out an integer operation according to a decoded result of said instruction decoder,

said memory operation unit retaining an instruction in a loop of instructions corresponding to a repeat instruction in a dedicated register in said register file when said repeat instruction is executed, and executing the loop of instructions while fetching the instruction retained in said dedicated register;

wherein said memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank to be accessed in a following pipeline cycle and a pipeline cycle corresponding to an access to an instruction memory bank without any accesses to other instruction memory banks ~~instruction readout only from said selected instruction memory bank without reading out any instruction from unselected instruction banks~~ to carry out a low power consumption pipeline process when fetching an instruction from said plurality of instruction memory banks.

11. (Original) The data processing apparatus according to claim 10, wherein said register file comprises a processor status word,

wherein said memory operation unit sets a flag in said processor status word at a first execution cycle of said loop, and retains, in the register of said register file, the instruction in the loop of instructions fetched from said instruction memory when said repeat instruction is executed, and

resets said flag in said processor status word at a second execution cycle of said loop, and executes said loop while fetching the instruction retained in said dedicated register.

12. (Previously Presented) The data processing apparatus according to claim 10, wherein said memory operation unit retains a plurality of instructions in the loop of instructions, in a plurality of dedicated registers in said register file when said repeat instruction is executed, and executes said loop of instructions while fetching said plurality of instructions retained in said plurality of dedicated registers.

13. (Previously Presented) The data processing apparatus according to claim 12, wherein said register file includes a processor status word, and

wherein said memory operation unit sets a flag in said processor status word at a first execution cycle of said loop, and retains the plurality of instructions in the loop of instructions fetched from said instruction memory in said plurality of registers, and resets said flag in said processor status word at a second execution cycle of said loop, and executes said loop while fetching said plurality of instructions retained in said plurality of dedicated registers.

Claim 14. (Cancelled)

15. (Previously Presented) The data processing apparatus according to claim 10, wherein said instruction memory further comprises a first bank select circuit decoding an address including a low order address to generate chip select signals of said plurality of instruction

memory banks so that a different instruction memory bank of said plurality of instruction memory banks is accessed when instructions at continuous addresses are accessed.

16. (Previously Presented) The data processing apparatus according to claim 10, wherein said data memory includes a plurality of data memory banks,

wherein said memory operation unit generates a pipeline cycle corresponding to selection of a data memory bank and a pipeline cycle corresponding to data access to carry out a pipeline process when said plurality of data memory banks are accessed.

17. (Original) The data processing apparatus according to claim 16, wherein said data memory further comprises a second bank select circuit decoding an address including a high order address to generate chip select signals of said plurality of data memory banks in order to divide said plurality of data memory banks into two different regions.

18. (Original) The data processing apparatus according to claim 17, wherein said second bank select circuit decodes an address including a low order address to generate a chip select signal of said plurality of data memory banks so that a different data memory bank in said plurality of data memory banks is accessed when data at continuous addresses in said two different regions are accessed.

19. (Original) The data processing apparatus according to claim 10, wherein said memory operation unit saves a plurality of registers including said dedicated register and switches a task in a task switch operation.